WHAT IS CLAIMED IS:

1. A processing system for an imager device comprising in an integrated, monolithic system:

a two-dimensional array source of imager signals;

a correlated double sample (CDS) circuit for receiving imager signals;

a variable gain amplifier (VGA) circuit configured to be selectably settable at one of a plurality of predetermined data resolution levels;

an analog-to-digital converter (ADC) having a selectable bit-width output and coupled to said VGA circuit;

a black level clamp connected to said ADC;

a gain circuit coupled to said ADC, said gain circuit configured to produce an output signal of selected magnitude;

a compander connected to said gain circuit and configured to receive a digital input of predetermined bit-width and to produce a digital output of selectably reduced bit-width; and

horizontal and vertical timing circuitry configured to control receipt of pixel intensity signals from a two-dimensional array source.

2. A processing system according to claim 1, including a multiplexer connected to said compander and said gain circuit, enabling selection between outputs of said gain circuit and said compander.

3. A processing system according to claim 1 wherein said VGA includes at least a single amplifier which is settable between first and second predetermined current levels.

4. A processing system according to claim 1 comprising a programmable timing generator.

5. A processing system according to claim 1 further including a serial interface connected to said black level circuit configured to be externally controllable to permit user control of black level settings.

6. A processing system according to claim 5, wherein said serial interface is connected to said horizontal and vertical timing circuitry and is adapted to be externally controllable to permit user control of selected horizontal and vertical timing factors.

7. The processing system according to claim 1 first and second digital-to-analog converters respectively adapted to produce analog currents of selected magnitude for meeting corresponding first and second imager device bias voltages.

8. A processing system for an imager device comprising on a single chip:

a two-dimensional array source of imager signals;

a correlated double sample (CDS) circuit for receiving imager signals;

a variable gain amplifier (VGA) circuit configured to be selectably settable at one of a plurality of predetermined data resolution levels;

an analog-to-digital converter (ADC) having a selectable bit-width output and coupled to said VGA circuit;

a black level clamp connected to said ADC;

a gain circuit coupled to said ADC, said gain circuit configured to produce an output signal of selected magnitude;

a compander connected to said gain circuit and configured to receive a digital input of predetermined

bit-width and to produce a digital output of selectably reduced bit-width; and

horizontal and vertical timing circuitry configured to control receipt of pixel intensity signals from a two-dimensional array source, wherein said VGA includes at least a single amplifier which is settable between first and second predetermined current levels.

9. A processing system according to claim 8 further including a serial interface connected to said black level circuit configured to be externally controllable to permit user control of black level settings, and wherein said serial interface is connected to said horizontal and vertical timing circuitry and is adapted to be externally controllable to permit user control of selected horizontal and vertical timing factors.

10. The processing system according to claim 8 first and second digital-to-analog converters respectively adapted to produce analog currents of selected magnitude for meeting corresponding first and second imager device bias voltages.

11. A processing system for an imager device comprising:

a two-dimensional array source of imager signals;

a correlated double sample (CDS) circuit for receiving imager signals;

a variable gain amplifier (VGA) circuit configured to be selectably settable at one of a plurality of predetermined data resolution levels;

an analog-to-digital converter (ADC) having a selectable bit-width output and coupled to said VGA circuit;

a black level clamp connected to said ADC;

a gain circuit coupled to said ADC, said gain circuit configured to produce an output signal of selected magnitude;

a compander connected to said gain circuit and configured to receive a digital input of predetermined bit-width and to produce a digital output of selectably reduced bit-width; and

horizontal and vertical timing circuitry configured to control receipt of pixel intensity signals from a two-dimensional array source, wherein said VGA includes at least a single amplifier which is settable between first and second predetermined current levels.

12. A processing system according to claim 11 further including a serial interface connected to said black level circuit configured to be externally controllable to permit user control of black level settings, and wherein said serial interface is connected to said horizontal and vertical timing circuitry and is adapted to be externally controllable to permit user control of selected horizontal and vertical timing factors, and further comprising first and second digital-to-analog converters respectively adapted to produce analog currents of selected magnitude for meeting corresponding first and second imager device bias voltages.

13. The processing system according to claim 12 wherein said serial interface is configured to enable user control of said first and second digital-to-analog converters.

14. A method for processing image signals, comprising:

producing an image signal;

amplifying said image signals at a selected drive current level; and

converting said image signals into digital signals having a selected resolution level.

15. The method according to claim 14 including selecting a drive current level to produce an selected resolution digital image.

16. The method according to claim 15 wherein said selected resolution digital image is a still image.

17. The method according to claim 16 including selecting a reduced drive current level to produce a video digital image.

18. A processing system for an imager device comprising:

a camera system for producing an imager signal;

a correlated double sample (CDS) circuit for receiving data from an imager;

a variable gain amplifier (VGA) circuit configured to be selectably settable at one of a plurality of predetermined data resolution levels;

an analog-to-digital converter (ADC) having a selectable narrow bit-width output and coupled to said VGA circuit;

a gain circuit coupled to said ADC, said gain circuit configured to produce an output signal of selected magnitude; and

a compander coupled to said gain circuit for reducing the bit-width of the output signal produced by said gain circuit.